National Semiconductor

September 2005

LMS4684
0.5Ω Low-Voltage, Dual SPDT Analog Switch

General Description

The LMS4684 is a low on-resistance, low voltage dual SPDT (Single-Pole/Double-Throw) analog switch that operates from a 1.8V to 5.5V supply. The LMS4684 features a 0.5Ω R_{ON} for its NC switch and 0.8Ω R_{ON} for its NO switch at a 2.7V supply. The digital logic inputs are 1.8V logic-compatible with a 2.7V to 3.3V supply and features break-before-make switching action.

The LMS4684 is available in the 12-bump micro SMD and the 10-lead LLP miniature packages. These PCB real estate saving packages offer extreme performance while saving money with small footprints.

Features

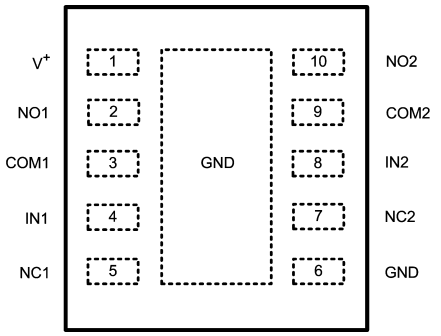
- NC switch R_{ON} 0.5Ω max @ 2.7V
- NO switch R_{ON} 0.8Ω max @ 2.7V
- 5 nA (typ) supply current T_A = 25˚C
- 1.8 to 5.5V single supply operation
- 12-Bump micro SMD package
- LLP-10 package, 3x4mm

Applications

- Power routing
- Battery-operated equipment
- Communications circuits
- Modems
- Cell phones

Connection Diagrams

10-LLP Package



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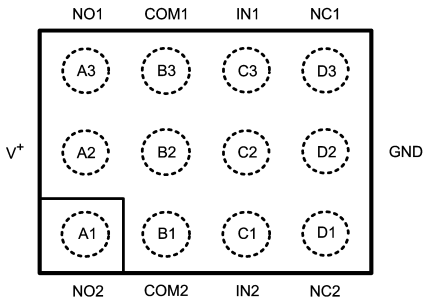
Exposed pad on back of package needs to be connected to pin 6 on the board

Top View

12-Bump micro SMD Package



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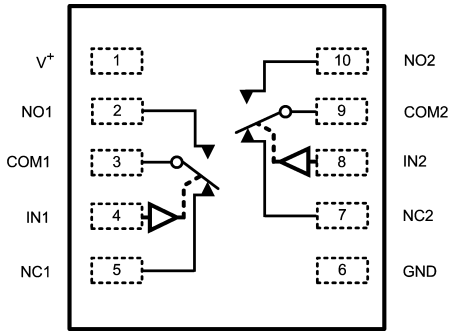
Center Bumps B2 and C2 are Not Electrically Connected

Top View
(Bumped Side Down)

Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
12-Bump micro SMD	LMS4684ITL	F09A	250 Units Tape and Reel	TLA12DPA
	LMS4684ITLX		3k Units Tape and Reel	
10-Pin LLP	LMS4684LD	L4684	1k Units Tape and Reel	LDA10B
	LMS4684LDX		4.5k Units Tape and Reel	

Schematic Diagram



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IN	NO	NC
0	Off	On
1	On	Off

Switches shown for Logic "0" input

Pin Descriptions

Name	Pin ID		Description
	LLP	micro SMD	
NC	5, 7	D3, D1	Analog switch normally closed terminal
IN	4, 8	C3, C1	Digital control input
COM	3, 9	B3, B1	Analog switch common terminal
NO	2, 10	A3, A1	Analog switch normally open terminal
V^+	1	A2	Positive supply voltage
GND	6	D2	Ground
		B2, C2	Not electrically connected. Can be used to help dissipate heat by connecting to GND pin.

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V^+	−0.3V to 6.0V
IN	−0.3V to 6.0V
COM, NO, NC	−0.3V to (V^+ + 0.3V)
Continuous Switch Current	±400 mA
ESD Tolerance (Note 3)	
Human Body Model	2000V
Machine Model	200V
Storage Temperature Range	−65˚C to 150˚C
Junction Temperature (Note 4)	150˚C Max

Operating Ratings (Notes 1, 2)

Nominal Supply Voltage	1.8V to 5.5V
IN Voltage (regardless of supply)	−0.3V to 5.5V
Temperature Range	−40˚C to 85˚C

Package Thermal Resistance

Package	θ_{J-A}
LLP-10	43˚C / W
micro SMD-12	57˚C / W

Electrical Characteristics

Unless otherwise specified, V^+ = 2.7 to 3.3V, V_{IH} = 1.4V, V_{IL} = 0.5V. Typical values are measured at 3V, and T_J = 25˚C. **Boldface** limits apply at temperature extremes.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{NO}, V_{NC}, V_{COM}	Analog Signal Range			0		V^+	V
$R_{ON\ (NC)}$	NC On-Resistance (Note 6)	V^+ = 2.7V, I_{COM} = 100 mA, V_{NC} =0 to V^+			0.3	**0.5**	Ω
$R_{ON\ (NO)}$	NO On-Resistance (Note 6)	V^+ = 2.7V, I_{COM} = 100 mA, V_{NO} =0 to V^+			0.45	**0.8**	Ω
ΔR_{ON}	On-Resistance Match Between Channels (Note 6), (Note 7)	V^+ = 2.7V, I_{COM} = 100 mA, V_{NC} or V_{NO} =1.5V			1.11	**60**	mΩ
$R_{FLAT(NC)}$	NC-On-Resistance Flatness (Note 8)	V^+ = 2.7V, I_{COM} = 100 mA, V_{NC} = 0 to V^+	LLP T_J = -40˚C to 85˚C		0.1	0.25	Ω
			micro SMD T_J = -40˚C to 85˚C		0.1	0.25	
$R_{FLAT(NO)}$	NO On-Resistance Flatness (Note 8)	V^+ = 2.7V, I_{COM} = 100 mA, V_{NO} = 0 to V^+			0.18	**0.35**	Ω
$I_{NO(OFF)}$ or $I_{NC(OFF)}$	NO or NC Off Leakage Current	V^+ = 3.3V, V_{NO} or V_{NC} = 3V, 0.3V; V_{COM} = 0.3V, 3V		−1	0.014	1	nA
				−10		**10**	
I_{COM} (ON)	COM On Leakage Current	V^+ = 3.3V, V_{NO} or V_{NC} = 3V, 0.3V, or floating; V_{COM} = 3V, or floating		−2		2	nA
				−20		**20**	
Dynamic Characteristics							
t_{ON}	Turn-On Time	V^+ = 2.7V, V_{NO} or V_{NC} = 1.5V; R_L = 50Ω; C_L = 35 pF;			38	60	ns
						70	
t_{OFF}	Turn-Off Time	V^+ = 2.7V, V_{NO} or V_{NC} = 1.5V; R_L = 50Ω; C_L = 35 pF;			22	40	ns
						50	
t_{BBM}	Break-Before-Make Delay	V^+ = 2.7V, V_{NO} or V_{NC} = 1.5V; R_L = 50Ω; C_L = 35 pF;		**2**	15		ns
Q	Charge Injection	COM = 0; R_S = 0; C_L= 1 nF;			200		pC
V_{ISO}	Off-Isolation (Note 5)	R_L = 50Ω; C_L= 5 pF; f = 100 kHz			-68		dB
V_{CT}	Crosstalk				-72		dB
Digital I/O							
V_{IH}	Input Logic High			**1.4**			V
V_{IL}	Input Logic Low					**0.5**	V
I_{IN}	IN Input Leakage Current	V_{IN} = 0 or V^+		**−1**		**1**	µA

Electrical Characteristics (Continued)

Unless otherwise specified, V^+ = 2.7 to 3.3V, V_{IH} = 1.4V, V_{IL} = 0.5V. Typical values are measured at 3V, and T_J = 25˚C. **Boldface** limits apply at temperature extremes.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Power Supply						
V^+	Power-Supply Range		**1.8**		**5.5**	V
I+	Supply Current	V+ = 5.5V		5		nA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed.

Note 2: All voltages are with respect to GND, unless otherwise specified.

Note 3: Human body model: 1.5 kΩ in series with 100 pF. Machine model, 0Ω in series with 200 pF.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} and T_A.

Note 5: Off-isolation = 20 $\log_{10}(V_{COM}/ V_{NO})$, where V_{COM} = output, V_{NO} = input switch off.

Note 6: Guaranteed by design.

Note 7: ΔR_{ON} is equal to the difference between NC1/NC2 R_{ON} or NO1/NO2 R_{ON} at a specified voltage.

Note 8: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

Parametric Measurement Information

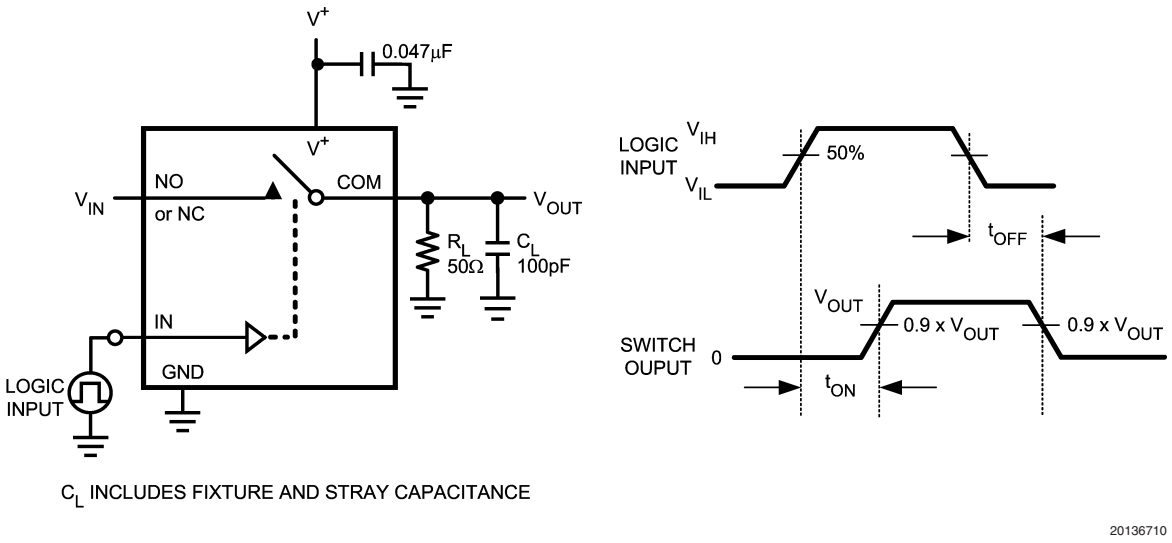


FIGURE 1. t_{ON} / t_{OFF} Time

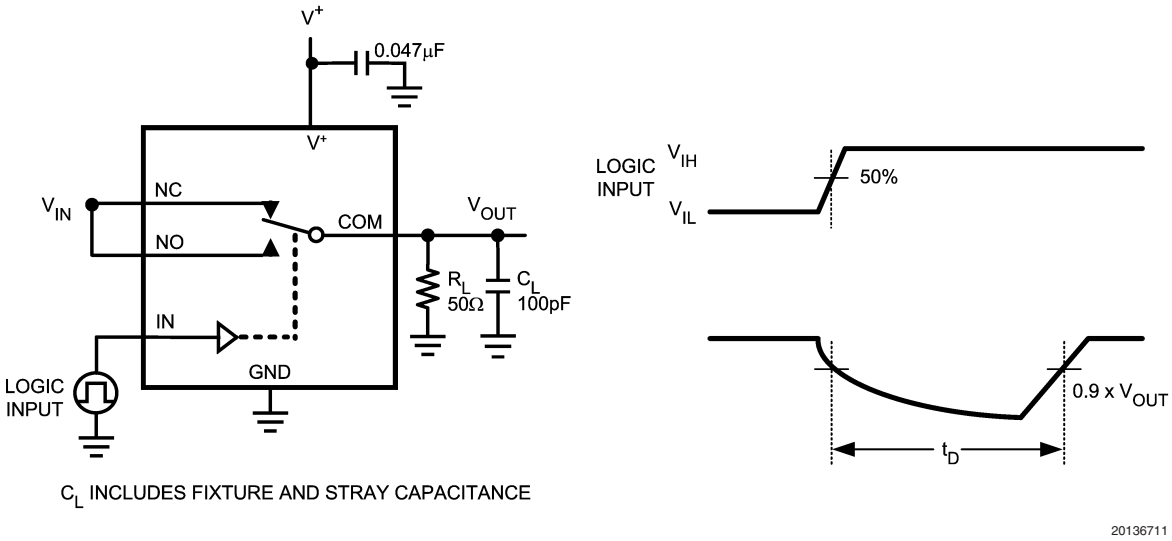


FIGURE 2. Break-Before Make Delay

Parametric Measurement Information (Continued)

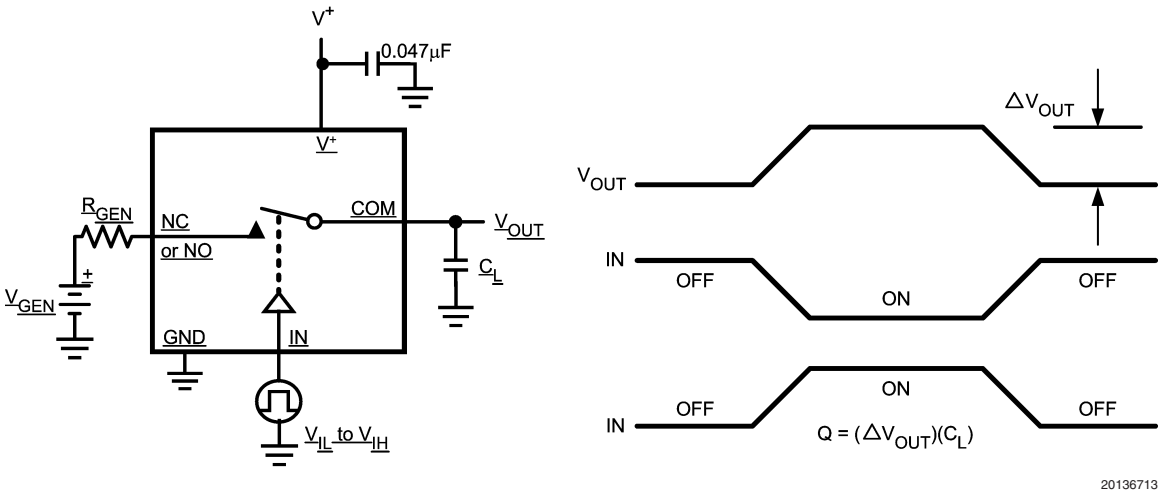


FIGURE 3. Charge Injection

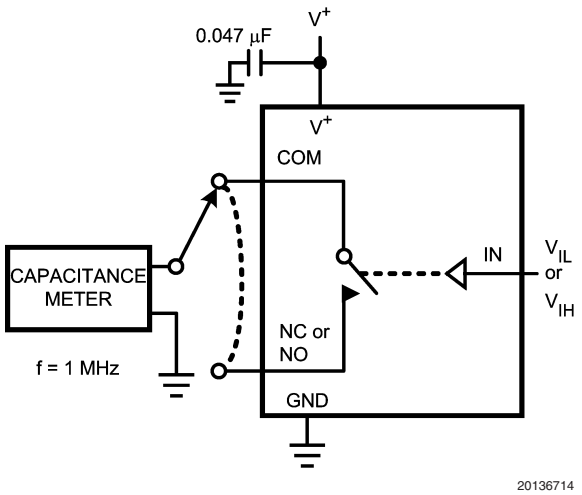
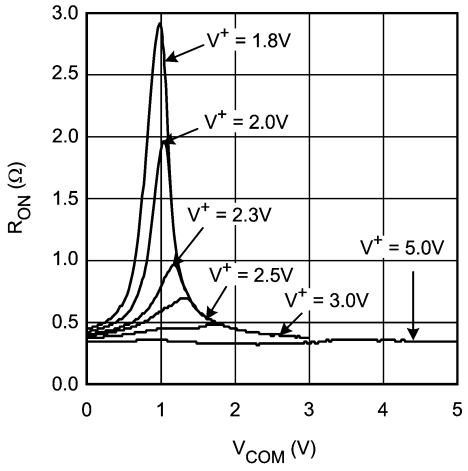


FIGURE 4. Channel Capacitance

Typical Performance Characteristics

NO ON Resistance vs. COM Voltage



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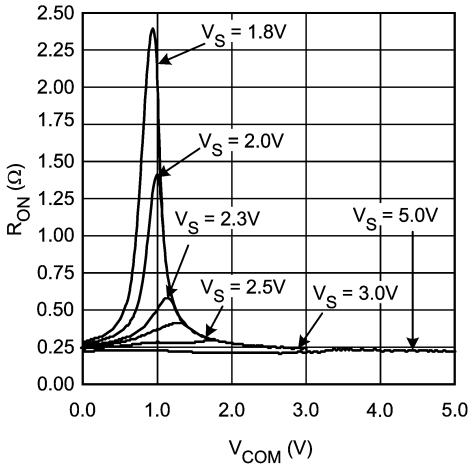
NC ON Resistance vs. COM Voltage



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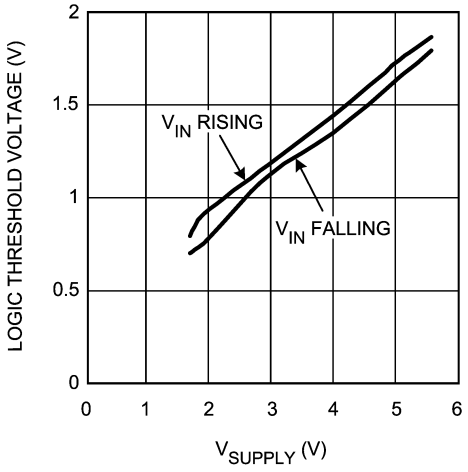
Logic Threshold Voltage vs. Supply Voltage



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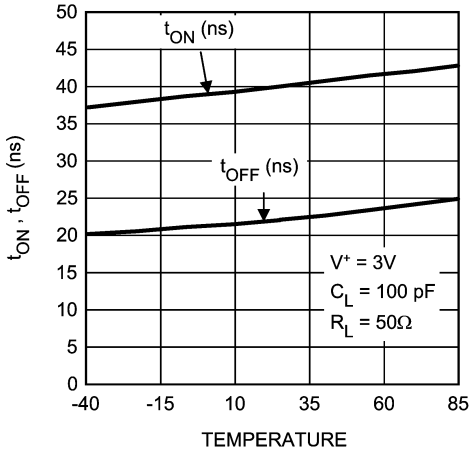
Turn-on / Turn-off Times vs. Temperature



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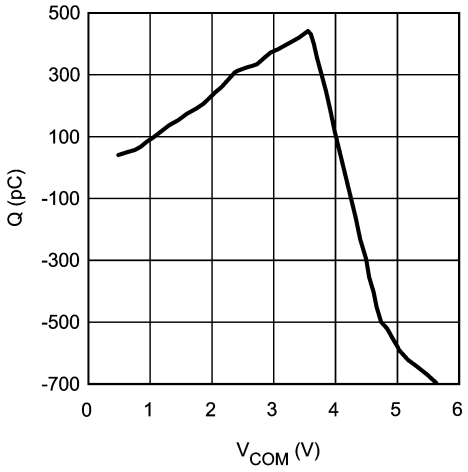
Charge Injection vs. COM Voltage



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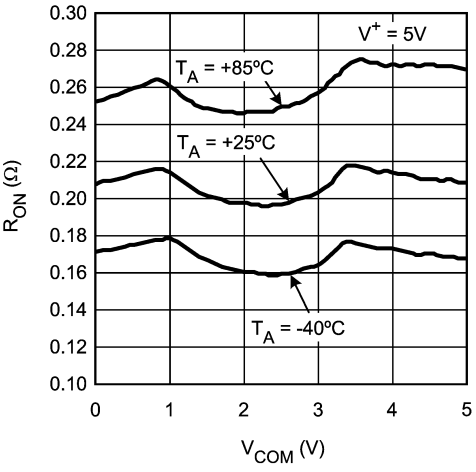
NC On-Resistance vs. COM Voltage



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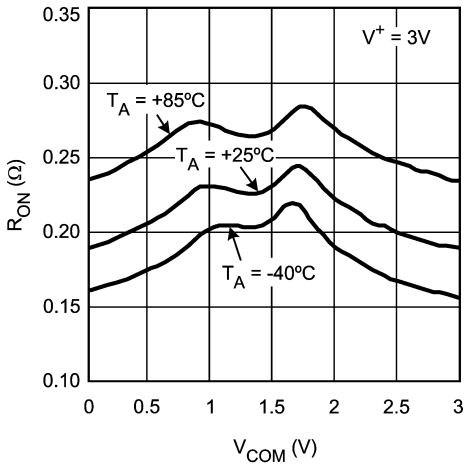
Typical Performance Characteristics (Continued)

NC On-Resistance vs. COM Voltage



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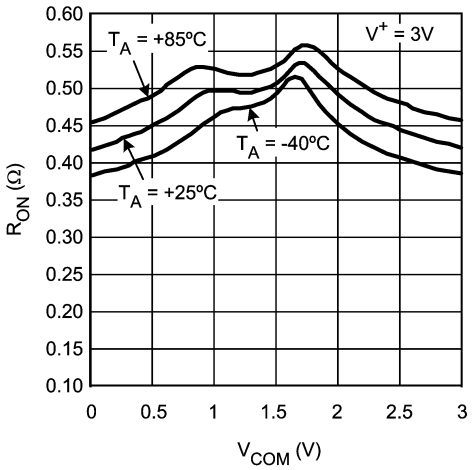
NO On-Resistance vs. COM Voltage



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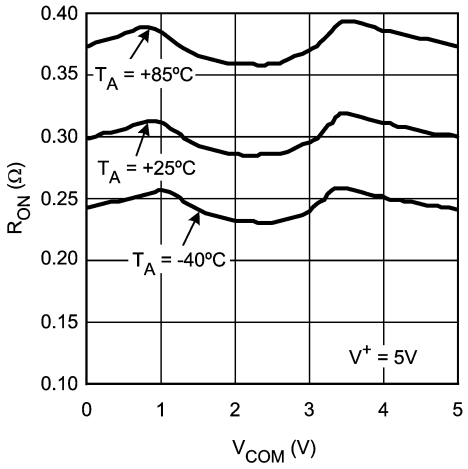
NO On-Resistance vs. COM Voltage



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Functional Description

The LMS4684 is a low voltage dual, extremely low On-Resistance analog switch that can operate over a supply voltage range of 1.8V to 5.5V. The LMS4684 has been fully characterized to operate in applications with 3V nominal supply voltage and features very low on resistance and fast Turn-Off and Turn-On times with break-before-make switching.

The switch operates asymmetrically; one terminal is normally closed (NC) and the other terminal normally open (NO).

Both NC and NO terminals are connected to a common terminal (COM). This configuration is ideal for applications with asymmetric loads such as speaker handsets and internal speakers.

Applications Information

1.0 ANALOG INPUT SIGNAL

Analog input signals can range from GND to V^+ and are passed through the switch with very little change. Each switch is bidirectional so any pin can be an input or output.

Exercise care when making connection to an inductive load, such as a motor. As is true with any analog switch used with an inductive load, the back emf produced when the switch is turned off can damage the LMS4684 by electrical overstress. For such applications, a diode should be connected across the motor to prevent damage to the switch, as indicated in *Figure 5*. Be sure the diode has adequate current carrying capabilities.

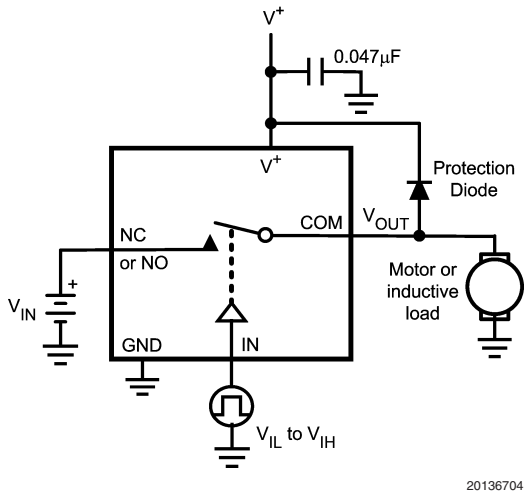


FIGURE 5. Inductive Load Over-Voltage Protection

2.0 DIGITAL CONTROL INPUTS

The IN pin can be driven to 5.5V regardless of the voltage level of the supply pin V^+. For example, if the LMS4684 is operated with a supply of 2V, the digital control input could still be driven to 5V. Power consumption is increased when the control pin is driven rail-to-rail.

3.0 SUPPLY VOLTAGE

It is good general practice to first apply the supply voltage to a CMOS device before sriving any other pins. This is also true for the LMS4684 analog switch, which is a CMOS device.

However, if it is necessary to have an analog signal applied before the supply voltage is applied and the analog signal source is not limited to 20 mA max, a diode connected between the supply voltage and the V^+ pin as shown in *Figure 6* will provide input protection. This will limit the max analog voltage to a diode drop below V^+. This diode, D1, will also provide protection against some over voltage situations.

It is also good practice to provide adequate supply bypassing to all analog circuits. We recommend a that minimum bypass capacitor value of 0.047µF be provided for the LMS4684. An inadequate bypass capacitor can lead to excessive supply current.

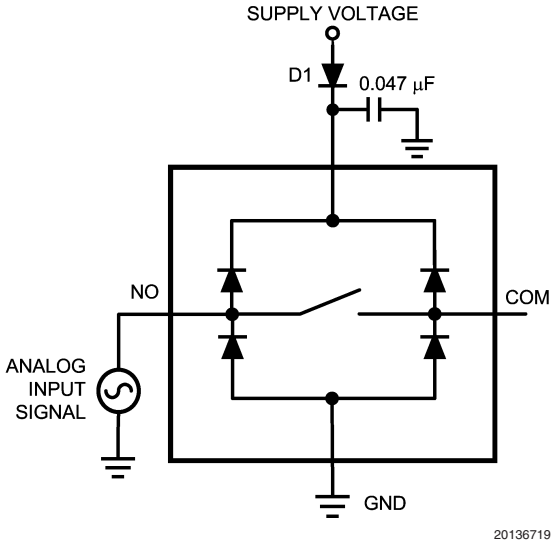


FIGURE 6. Input Over Voltage Protection Circuitry

4.0 OFF-ISOLATION

Analog switches are composed of FETs (field Effect Transistors). The channel resistance is low when the pass transistors are "on" and that resistance is high when the pass transistors are "off". However, when the pass transistors are "off", the source to drain capacitance of the pass transistors will pass some energy. This capacitance is inversely proportional to the switch "on" resistance, so a switch with a low "on" resistance may not be suitable for some high frequency applications.

Figure 7 shows the equivalent circuit of an analog switch. Unless the load impedance after the switch is relatively low, the switch capacitance will couple excessive energy across the "open" switch at higher frequencies, degrading off isolation performance. Off Isolation of the LMS4684 is specified with a 50Ω load. Higher load impedances will degrade off isolation performance compared with what is specified.

Applications Information (Continued)

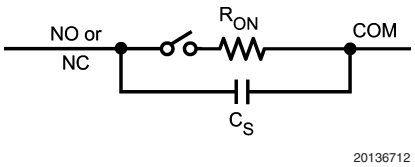


FIGURE 7. Equivalent Circuit of an Analog Switch

Off isolation may be improved by decreasing the LMS4684 load impedance below 50Ω. When doing this, be sure that the LMS4684 maximum current rating is not exceeded. Also, decreasing the load impedance too much can result in excessive signal distortion because the channel resistance variation with input signal voltage would then be a greater percentage of the load impedance.

If it is desired to extend the usable bandwidth of the LMS4684 while maintaining reasonable off-isolation is through the use of the circuit of *Figure 8*.

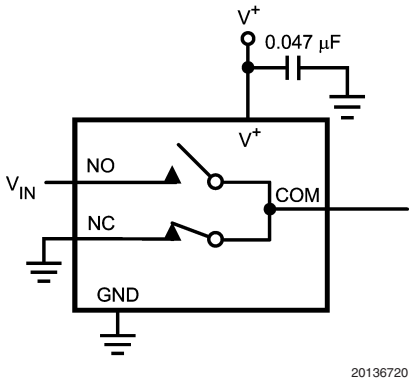


FIGURE 8. Using the LMS4684 at higher frequencies

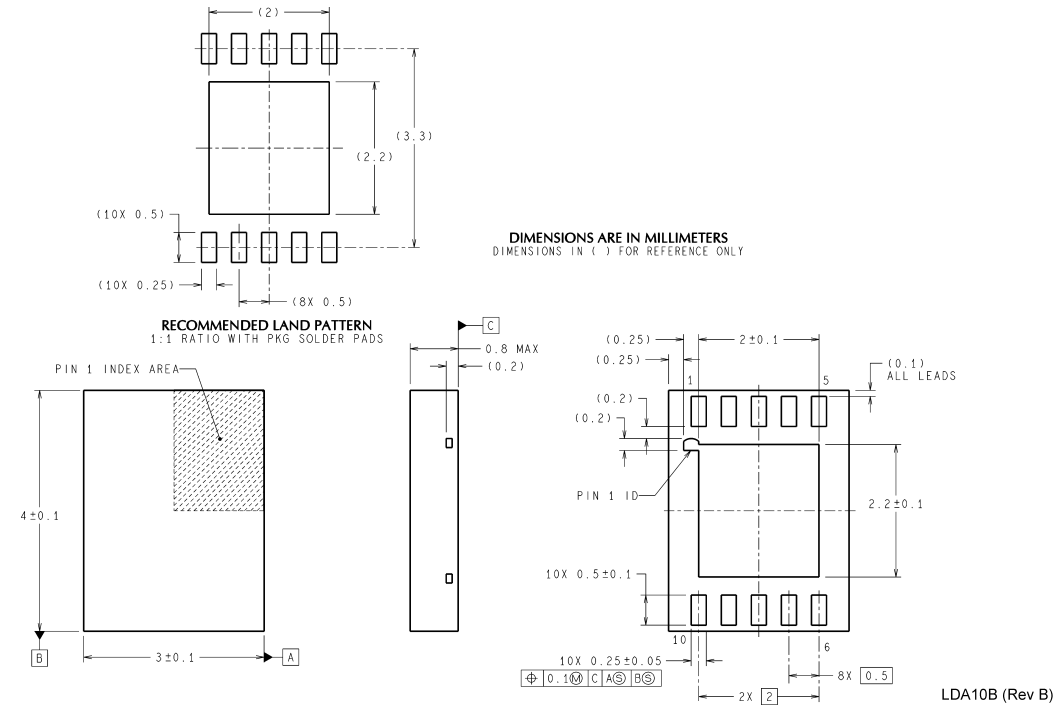
5.0 PCB LAYOUT AND THERMAL CONSIDERATIONS

Both the LLP and micro SMD packages offer enhanced board real estate savings because of their small footprints. These tiny packages are capable of handling high continuous currents because of the advanced package thermal handling capabilities.

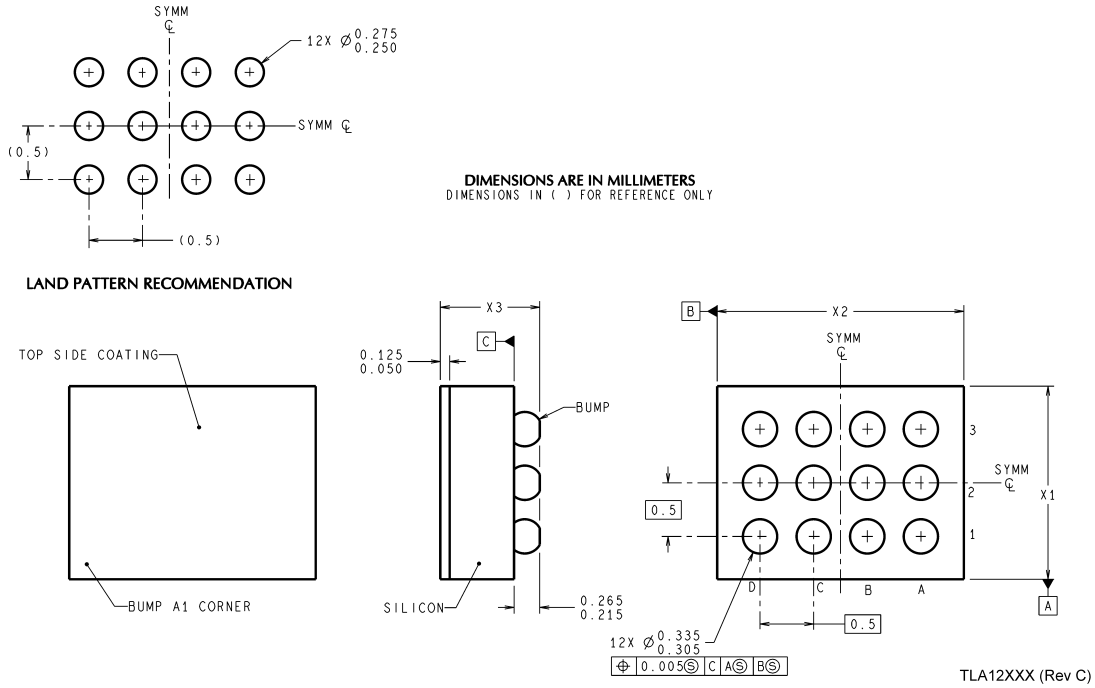
The LLP package has the exposed die attach pad internally connected to the internal circuit GND. When this pad is soldered to copper on the PCB board according to Application Note AN-1187, the full thermal capability of the LLP package can be achieved without additional bulky heat sinks to dissipate the heat generated. The micro SMD package has a similar capability to dissipate heat through Bumps B2 and C2, which are not electrically connected. To enhance heat dissipation of the micro SMD package B2 and C2 could be connected to the GND pin through copper traces on the board.

See Application Note AN-1112 for micro SMD package considerations.

Physical Dimensions inches (millimeters) unless otherwise noted



10-Lead LLP
NS Package Number LDA10B



X1 = 1590 ± 30 µm; X2 = 2327 ± 30 µm; X3 = 600 ± 75 µm

12-Bump micro SMD
NS Package Number TLA12DPA

Notes

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